UNIPLANAR MMICs AND THEIR APPLICATIONS

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ABSTRACT

Key uniplanar MMICs for a 26GHz full MMIC receiver have been designed and fabricated using 0.3um-gate ion implanted GaAs IC processes. They consist of coplanar waveguides, slotlines, and lumped circuit elements (GaAs FETs, capacitors, etc.), which employ only one side of GaAs substrate and have no via holes and no polished thin substrates. The developed uniplanar MMICs yield improved RF performance, chip size reduction, and fabrication process simplification.

1. Introduction

The research and development of monolithic microwave integrated circuits (MMICs) has progressed remarkably in the last several years [1],[2]. Most of these MMICs consist of microstrip line configurations. These required the following additional processes besides those of GaAs FET; via holes to connect the GaAs FETs with the ground conductors, and thin substrate with accurate thickness to adjust the characteristic impedance. In order to reduce these additional manufacturing steps and to reduce chip size of MMICs, a "uniplanar" circuit configurations for MMICs which was named "uniplanar MMICs" was proposed by the authors [3]. Uniplanar MMICs use only one side of the substrate, unlike microstrip line based MMICs with strip lines on one surface and the ground on the back surface.

In this paper, key circuits for a 26GHz full MMIC receiver have been designed and fabricated using uniplanar circuit configurations. These uniplanar MMICs play an important role in subscriber radio systems and satellite communication systems, particularly in reducing size and cost.

2. Uniplanar MMIC features and key circuits for a 26GHz receiver

Uniplanar MMICs consist of coplanar waveguides (CPWs), slotlines, and lumped circuit elements such as FETs, diodes, resistors, capacitors, and inductors, which are all on one side of the GaAs substrate. The uniplanar MMIC has the following advantages [3],[4]: (A) RF and DC grounding of the active devices are easily made without use of via holes and substrate thinning.

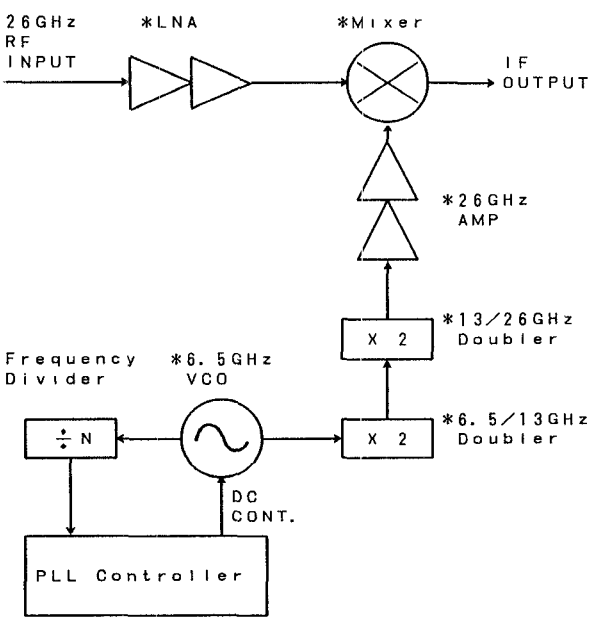

Fig. 1. Block diagram of a 26GHz full MMIC receiver module.
* indicates the uniplanar MMICs developed in this paper.

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(B) The CPW reduces coupling effects between adjacent lines. This results in very compact design. (C) The combination of CPW (unbalanced line) and slotline (balanced line) offers simple and compact balance/unbalance circuits. (D) RF performance of MMICs are measured easily on a wafer by using Cascade-microtech's probe heads.

The system block diagram of a 26GHz receiver module using a phase locked loop local oscillator is shown in Fig.1. The following indispensable circuits for a 26GHz full MMIC receiver were designed and fabricated by using newly proposed uniplanar MMICs; 26GHz low noise amplifiers (LNA), 26GHz medium power amplifiers, 6.5GHz dual output voltage controlled oscillators (VCO), 6.5/13GHz frequency doublers, 13/26GHz frequency doublers, and 26GHz/1GHz FET mixers.

All uniplanar chips were fabricated using advanced SAINT (self-aligned implantation for n^+-layer technology) processes which were self-aligned ion implantation processes developed in our laboratories[5]. GaAs advanced SAINT FETs in these uniplanar MMICs have 0.3um gate length, maximum oscillation frequency of more than 60GHz and a noise figure of 2.0dB at 20GHz.

3. 26GHz LNA and 26GHz medium power amplifier

A photograph of the two-stage monolithic LNA using CPWs is shown in Fig.2. The optimum circuit element values for a noise match at 26GHz were obtained on the basis of measured S-parameters and four noise parameters of the FETs by using the Super Compact program. The measured and calculated gain and noise figure are shown in Fig.3. Here, Ls denotes FET source inductances due to the connection of the source and ground. Ls degrades the gain performance in FET amplifiers especially at high frequency. As Ls in a CPW amplifier is fairly smaller than that in a microstrip line (MSL) based amplifier, the CPW amplifier is expected to have better RF performance than the MSL amplifier. The CPW LNA had a measured noise figure of 3.6dB with a gain of 7.3dB at 26GHz. This is the best noise figure value for K-band monolithic LNAs ever reported.

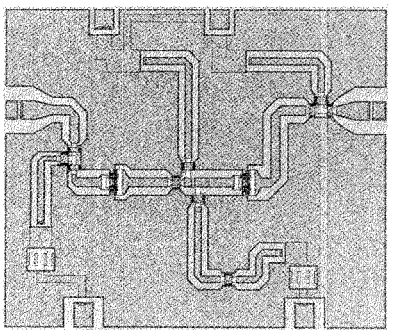

Fig. 2. Photograph of the 26GHz two-stage monolithic low noise amplifier using CPWs.
(Chip size: 1.28 x 1.55 mm)

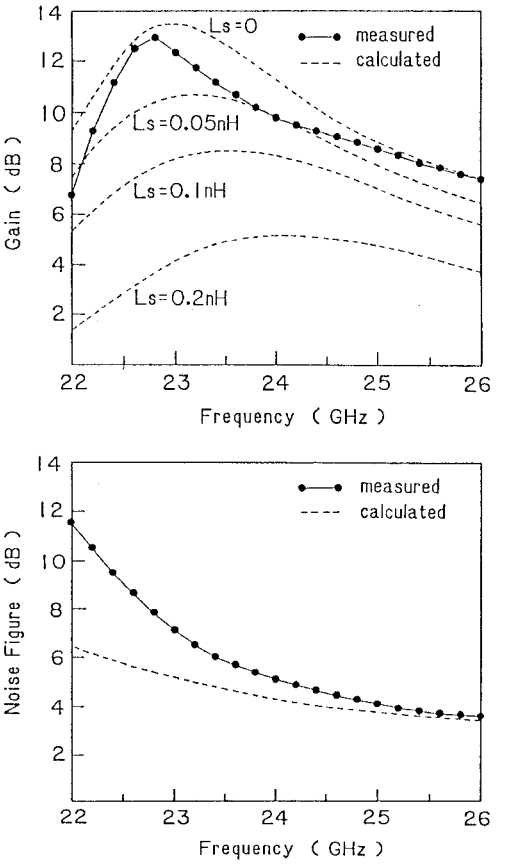

Fig. 3. Measured and calculated gain and noise figure of the CPW monolithic LNA. Calculated gain is shown with a parameter of FET source inductance.

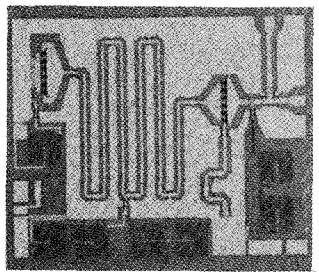

Fig. 4. Photograph of the 6.5GHz dual output monolithic VCO using CPWs. (Chip size: 1.97 x 1.60mm)

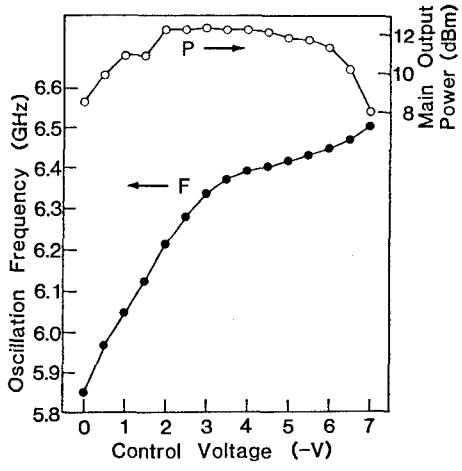

Fig. 5. Measured performance of the dual output VCO. The sub output power was about 0dBm.

The 26GHz CPW two-stage medium power amplifier was also developed. The chip size was only 1.14 x 1.28 mm. Measured gain was 6.7dB with output power of 14dBm at 26GHz.

4. 6.5GHz dual output VCO

A photograph of the 6.5GHz dual output VCO using CPWs is shown in Fig.4. The transmission line design approach was employed since it provided more accurate design than the lumped element approach. Since the gate circuit required a CPW more than 6mm, meandering CPW layout was employed to reduce chip size. Chip size is only 1.97 x 1.60 mm. The CPW has a great advantage in a compact layout because of low coupling of adjacent lines. As control voltage varied from 0 to -7V, oscillation frequency varied from 5.9GHz to 6.5GHz as shown in Fig.5.

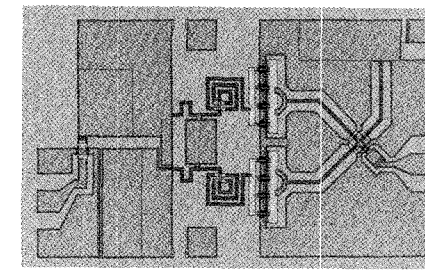

Fig. 6. Photograph of the monolithic 13/26GHz balanced frequency doubler using a combination of CPWs and slotlines. (Chip size: 1.2 x 0.8mm)

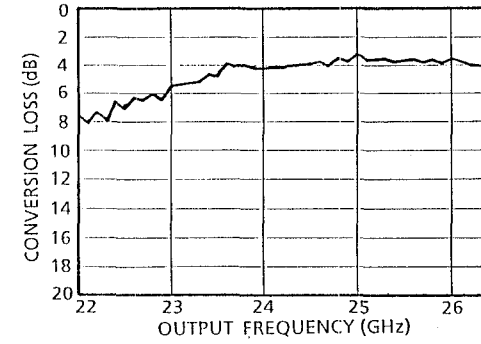

Fig. 7. Measured conversion loss of the 13/26GHz frequency doubler. The fundamental signal suppression was better than 30dB.

5. Balanced FET frequency doublers

A photograph of the 13GHz/26GHz balanced FET frequency doubler using CPWs and slotlines is shown in Fig. 6. The uniplanar circuit configuration provides very compact balanced circuits. Chip size is only 1.2 x0.8 mm. 13GHz input unbalanced signal fed in a coplanar input terminal was changed to a balanced signal through a CPW/SLOT transition. Then the signal was fed to two FETs through a lumped element matching network consisting of spiral inductors and MIM capacitor. Here, the two FETs were excited out-of-phase. The 26GHz output signal was combined in-phase and obtained from a CPW output terminal, while the 13GHz fundamental signal was canceled at the output terminal because of out-of-phase combining. The frequency dependence of conversion loss is shown in Fig.7. Measured conversion loss was

better than 4dB with the fundamental signal suppression of better than 30dB.

The 6.5GHz/13GHz balanced FET frequency doubler was also developed. Measured conversion loss was better than 0dB with the fundamental signal suppression of better than 20dB.

6. 26GHz/1GHz FET mixer

The FET mixer using drain local injection was developed. The mixer consists of an FET, MIM capacitors, CPWs, and air-bridges. It is characterized by simple and compact configuration. Chip size was only 1.0 x 1.0 mm as shown in Fig.8. Measured conversion loss was better than 5dB at 26GHz as shown in Fig.9.

7. Conclusion

Key uniplanar MMICs have been developed for a 26GHz full MMIC receiver. Uniplanar MMICs yield RF performance improvement, chip size reduction, and fabrication process simplification. Specially, the 26GHz monolithic LNA had a noise figure of 3.6 dB with a gain of 7.3dB at 26GHz. This noise figure is the best value in K-band monolithic LNAs ever reported. Total chip area of uniplanar MMICs for the 26GHz receiver module is predicted to be much smaller than that of microstrip line based MMICs. Such smaller size uniplanar MMICs which are fabricated by simpler processes without via holes and substrate thinning are promissing to have better yield and lower cost.

Acknowledgment

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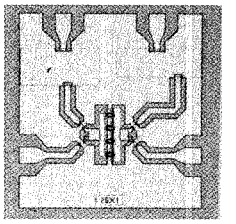

Fig. 8. Photograph of the 26GHz CPW FET mixer using drain local injection. (Chip size: 1.0 x 1.0mm)

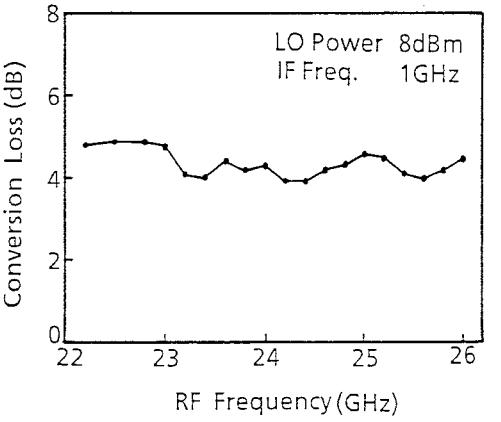

Fig. 9. Measured conversion loss of the CPW FET mixer.

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